What is claimed is:

1. A method for forming a titanium layer supported by a substrate, comprising:
forming a seed layer supported by the substrate by combining a first precursor with a first reducing agent; and
forming the titanium layer supported by the substrate by combining a titanium-containing precursor with the seed layer.

2. A method for forming a titanium layer supported by a substrate, comprising:
forming a seed layer supported by the substrate by combining a first precursor with a first reducing agent, wherein the first precursor is an alkane; and
forming the titanium layer supported by the substrate by combining a titanium-containing precursor with the seed layer.

3. The method of claim 1, further comprising annealing the titanium layer to form titanium silicide.

4. The method of claim 1, wherein forming a seed layer comprises forming a seed layer in accordance with the following chemical process (I):

(I) $MR_x + H_2 \rightarrow M + \text{alkanes},$

wherein: M is an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony;
R is an alkyl group; and
x is some integer value equal to the valence of M.

5. The method of claim 1, wherein forming a seed layer comprises forming a zinc seed layer in accordance with the following chemical process (I):

(I) $ZnR_2 + H_2 \rightarrow Zn + \text{alkanes},$

wherein: R is an alkyl group.

6. The method of claim 4, wherein forming a seed layer is performed at a temperature between approximately 100 and 600 degrees Celsius.

7. The method of claim 1, wherein forming the titanium layer comprises forming the titanium layer in accordance with the following chemical process (II):

(II) $TiCl_4 + M \rightarrow Ti + MCl_x$

wherein: M an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

x is some integer value equal to the valence of M.

8. The method of claim 1, wherein forming the titanium layer comprises forming the titanium layer in accordance with the following chemical process (II):

(II) $TiCl_4 + Zn \rightarrow Ti + ZnCl_2.$

9. The method of claim 7, wherein forming the titanium layer in accordance with chemical process (II) is performed at a temperature between approximately 100 and 600 degrees Celsius.

10. The method of claim 1, wherein forming the titanium layer further comprises forming titanium silicide.

11. The method of claim 10, wherein forming titanium silicide comprises forming titanium silicide at a temperature of between approximately 250 to 750 degrees Celsius.

12. The method of claim 1, wherein forming the titanium layer comprises forming the titanium layer comprising a titanium alloy.

13. The method of claim 12, wherein forming the titanium layer comprising a titanium alloy comprises a titanium alloy containing titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony.

14. The method of claim 12, wherein forming the titanium layer comprising a titanium alloy comprises a titanium alloy containing titanium and zinc.

15. A method for forming a titanium layer on an integrated circuit, comprising:
forming a seed layer on the integrated circuit by combining a first precursor with a reducing agent with chemical vapor deposition (CVD); and
forming the titanium layer on the integrated circuit by combining the seed layer with a second precursor with CVD;
wherein the seed layer is formed according to the following chemical process (I):

(I) $MR_x + H_2 \rightarrow M + \text{alkanes}$,

wherein: M an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony;
R is an alkyl group; and
x is some integer value equal to the valence of M;

wherein chemical process (I) is performed at a temperature greater than 400 degrees Celsius; and

wherein the titanium layer is formed according to the following chemical process (II):

(II) $TiCl_4 + M \rightarrow Ti + MCl_x$,

wherein chemical process (II) is performed at a temperature greater than 400 degrees Celsius.

16. A method for forming a titanium layer on an integrated circuit, comprising:

forming a seed layer on the integrated circuit by combining a first precursor with a reducing agent with chemical vapor deposition (CVD);

forming the titanium layer on the integrated circuit by combining the seed layer with a second precursor with CVD;

wherein the seed layer is zinc, and formed according to the following chemical process (I):

(I) $ZnR_2 + H_2 \rightarrow Zn + alkanes$,

wherein R is an alkyl group and chemical process (I) is performed at a temperature greater than 400 degrees Celsius; and

wherein the titanium layer is formed according to the following chemical process (II):

(II) $TiCl_4 + Zn \rightarrow Ti + ZnCl_2$,

wherein chemical process (II) is performed at a temperature greater than 400 degrees Celsius.

17. The method of claim 15, further comprising annealing the titanium layer to form titanium silicide.

18. The method of claim 15, wherein forming the titanium layer further comprises forming titanium silicide.

19. The method of claim 18, wherein forming the titanium silicide comprises forming titanium silicide at a temperature of between approximately 250 to 750 degrees Celsius.

20. The method of claim 15, wherein forming the titanium layer comprises forming the titanium layer comprising a titanium alloy.

21. The method of claim 15, wherein forming the titanium layer comprising a titanium alloy comprises a titanium alloy containing titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony.

22. The method of claim 15, wherein forming the titanium layer comprising a titanium alloy comprises a titanium alloy containing titanium and zinc.

23. A method for forming a titanium layer supported by a substrate, comprising:

forming a seed layer supported by the substrate by combining a first precursor with a first reducing agent, wherein the first precursor is an alkane and wherein the alkane comprises an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

forming the titanium layer supported by the substrate by combining a titanium-containing precursor with the seed layer.

24. A chemical vapor deposition method of providing a layer of titanium on an integrated circuit within a chemical vapor deposition (CVD) reactor, the method comprising:

injecting a first precursor and reducing agent in the CVD reactor;

forming a seed layer on the integrated circuit from reaction of the first precursor and the reducing agent, wherein the first precursor is an alkane;

injecting a second precursor in the CVD reactor; and

forming the titanium layer on the integrated circuit from reaction of the second precursor and the seed layer.

25. A chemical vapor deposition method of providing a layer of titanium on an integrated circuit within a chemical vapor deposition (CVD) reactor, the method comprising:

injecting a first precursor and reducing agent in the CVD reactor;

forming a seed layer on the integrated circuit from reaction of the first precursor and the reducing agent, wherein the first precursor is an alkane and wherein the alkane comprises an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony;

injecting a second precursor in the CVD reactor; and

forming the titanium layer on the integrated circuit from reaction of the second precursor and the seed layer.

26. A chemical vapor deposition method of providing a layer of titanium on an integrated circuit within a chemical vapor deposition (CVD) reactor, the method comprising:

injecting a first precursor and reducing agent in the CVD reactor;

forming zinc on the integrated circuit from a reaction of the first precursor and the first reducing agent;

injecting a second precursor in the CVD reactor; and

forming the titanium layer on the integrated circuit from a reaction of the second precursor and the zinc.

27. The method of claim 24, further comprising annealing the titanium layer to form titanium silicide.

28. The method of claim 24, wherein forming the seed layer is in accordance with the following chemical process (I):

(I) $MR_x + H_2 \rightarrow M + \text{alkanes},$

wherein: M is an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony;

R is an alkyl group; and

x is some integer value equal to the valence of M.

29. The method of claim 26, wherein forming the zinc is in accordance with the following chemical process (I):

(I) $ZnR_2 + H_2 \rightarrow Zn + \text{alkanes},$

wherein: R is an alkyl group.

30. The method of claim 28, wherein forming the seed layer comprises forming the seed layer according to chemical process (I) at a temperature between approximately 100 and 600 degrees Celsius.

31. The method of claim 28, wherein forming the titanium layer comprises forming the titanium layer in accordance with the following chemical process (II):

(II) $TiCl_4 + M \rightarrow Ti + MCl_x$

32. The method of claim 29, wherein forming the titanium layer comprises forming the titanium layer in accordance with the following chemical process (II):

(II) $TiCl_4 + Zn \rightarrow Ti + ZnCl_2$.

33. The method of claim 31, wherein forming the titanium layer comprises forming the titanium layer according to chemical process (II) at a temperature between approximately 100 and 600 degrees Celsius.

34. The method of claim 24, wherein forming the titanium layer further comprises forming titanium silicide.

35. The method of claim 34, wherein forming titanium silicide comprises forming titanium silicide at a temperature of between approximately 250 to 750 degrees Celsius.

36. The method of claim 24, wherein forming the titanium layer further comprises forming a titanium alloy containing titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony.

37. The method of claim 26, wherein forming the titanium layer further comprises forming a titanium zinc alloy layer.

38. A method for forming a titanium layer supported by a substrate, comprising forming the titanium layer according to the following chemical process (III):

(III) $TiCl_4 + M\,(source) \rightarrow Ti + MCl_x$

wherein: M is an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

x is some integer value equal to the valence of M.

39. A method for forming a titanium layer supported by a substrate, comprising forming the titanium layer according to the following chemical process (III):

(III) $TiCl_4 + Zn \rightarrow Ti + ZnCl_2$.

40. The method of claim 38, further comprising annealing the titanium layer to form titanium silicide.

41. A method for forming a titanium layer supported by a substrate, comprising forming the titanium layer according to the following chemical process (IV):

(IV) $MR_x + H_2 + TiCl_4 \rightarrow Ti + MCl_x +$ alkanes,

wherein: M is an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony;

R is an alkyl group; and

x is some integer value equal to the valence of M.

42. A method for forming a titanium layer supported by a substrate, comprising forming the titanium layer according to the following chemical process (IV):

(IV) $ZnR_2 + H_2 + TiCl_4 \rightarrow Ti + ZnCl_2 + \text{alkanes}$,

wherein: R is an alkyl group.

43. The method of claim 41, wherein forming the titanium layer comprises forming the titanium layer comprising a titanium alloy.

44. An integrated circuit comprising:

a layer of a titanium alloy, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the layer.

45. The integrated circuit of claim 34, wherein the titanium alloy comprises titanium and zinc.

46. A memory, comprising:

a memory array;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array; and

wherein the memory array, control circuit and I/O circuit each comprise:

a layer of a titanium alloy, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the layer.

47. The memory of claim 46, wherein the titanium alloy comprises titanium and zinc.

48. A contact, comprising:
a titanium alloy layer formed overlying walls of a contact hole; and
a titanium silicide layer formed overlying an exposed silicon base layer of the contact hole.

49. A contact, comprising:
a titanium alloy layer formed overlying walls of a contact hole, wherein the titanium alloy layer comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and
a titanium silicide layer formed overlying an exposed silicon base layer of the contact hole.

50. A contact, comprising:
a titanium alloy layer formed overlying walls of a contact hole, wherein the titanium alloy layer comprises titanium and zinc; and
a titanium silicide layer formed overlying an exposed silicon base layer of the contact hole.

51. A via, comprising:
a titanium alloy layer formed overlying walls and an exposed base layer of a contact hole; and
a fill coupled to the titanium alloy layer, wherein the fill comprises a metal selected from the group consisting of tungsten and aluminum.

52. The via of claim 51, wherein the titanium alloy layer comprises titanium and zinc.

53. A via, comprising:

a titanium alloy layer formed overlying walls and an exposed base layer of a contact hole, wherein the titanium alloy layer comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a fill coupled to the titanium alloy layer, wherein the fill comprises a metal selected from the group consisting of tungsten and aluminum.

54. The via of claim 51, further comprising a titanium nitride layer interposed between the titanium alloy layer and the fill.

55. A via, comprising:

a titanium alloy layer formed overlying walls and an exposed base layer of a contact hole;

a fill comprising a metal selected from the group consisting of tungsten and aluminum; and

a titanium nitride layer interposed between the titanium alloy layer and the fill.

56. A via, comprising:

a titanium alloy layer formed overlying walls and an exposed base layer of a contact hole, wherein the titanium alloy layer comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony;

a fill comprising a metal selected from the group consisting of tungsten and aluminum; and

a titanium nitride layer interposed between the titanium alloy layer and the fill.

57. A memory device, comprising:

a memory array;

a control circuit operatively coupled to the memory array; and

an I/O circuit operatively coupled to the memory array;

wherein at least one of the memory array, control circuit and I/O circuit comprises a contact having a titanium alloy layer formed overlying walls of a contact hole and a titanium silicide layer formed overlying an exposed silicon base layer of the contact hole.

58. A memory device, comprising:

a memory array;

a control circuit operatively coupled to the memory array; and

an I/O circuit operatively coupled to the memory array;

wherein at least one of the memory array, control circuit and I/O circuit comprises a via having a titanium alloy layer formed overlying walls and an exposed base layer of a contact hole and a fill coupled to the titanium alloy layer, wherein the fill comprises a metal selected from the group consisting of tungsten and aluminum.

59. A memory device, comprising:

a memory array;

a control circuit operatively coupled to the memory array; and

an I/O circuit operatively coupled to the memory array;

wherein at least one of the memory array, control circuit and I/O circuit comprises a titanium layer, wherein the titanium layer is produced using a method, the method comprising:

forming a seed layer supported by a substrate by combining a first precursor with a first reducing agent; and

forming the titanium layer supported by the substrate by combining a titanium-containing precursor with the seed layer.